REMARKS

This communication is in response to the Final Office Action of March 1, 2005. Claims 25-44 were rejected. Claims 25, 30, 37, and 41 were amended. Claims 25-44 are pending.

Applicant has amended independent claims 25, 30, 37, and 41 to include a limitation that the CPU must acquire access to the I/O bus in order to transfer vertex data across the I/O bus to the graphics accelerator. This amendment adds a limitation similar to remarks previously considered by the Examiner in the amendment filed on November 1, 2004 such that it is believed that this amendment raises no new substantive issues for the Examiner to consider.[1] Support for this amendment is, for example, also found on page 2, lines 20-22; page 6, line 21 to page 7, line 2; and page 7, line 20 to page 8, line 3.

Applicant notes that this amendment distinguishes the I/O bus of the claimed invention from point-to-point connections and pipeline architectures that do not require bus arbitration for a device to access the I/O bus. Referring to Figure 1 of Applicant's specification, in an exemplary embodiment a number of different devices can be connected to the I/O bus 13, such as for example a CPU 11 (e.g., via a bridge), graphics accelerator 15, and other I/O devices, such as two bus master/slave elements 14. In an I/O bus architecture capable of supporting three or more different devices a bus protocol (sometimes also known as a bus arbitration process) is commonly used to determine which device can access the bus at a particular point in time to make a data transfer.

In the Final Rejection of March 1, 2005, the Examiner rejected claims 25-44 under 35 U.S.C. 103(a) over Porterfield (U.S. Pat. No. 6,069,638) in view of Morgan (U.S. Pat. No. 5,821,940). The Examiner contends in sections 2-3 that the combination of the display list controller 16, transformation processor 18, cache storage means 22 and backend processor 24 of Morgan is a graphics accelerator. The Examiner stated in section 2 that it would have been obvious to combine the graphics accelerator of Morgan in the graphics system of Figure 1 of Porterfield, which has a processor, system bus, and graphics accelerator, in order to achieve Applicant's claimed invention. Applicant respectfully traverses the rejections.

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[1] See, e.g., pg. 8 of the Amendment of November 1, 2004, "since the I/O bus must be acquired to transfer data, the number of I/O bus acquisitions required to transfer vertex data to the graphics accelerator is reduced, which improves system performance."

The Examiner has cited no support, in Morgan, Porterfield, or other references, for a motivation for combining the teachings of the two references. In particular, the Examiner contends, without citing a reference, that one of ordinary skill in the art would have been motivated to combine the teachings of Porterfield and Morgan in order to reduce memory access bandwidth from system memory over the I/O bus. However, Morgan and Porterfield provide no such motivation for the combination.

Morgan is directed towards the problem of reducing processing time in a pipelined architecture, not solving bus bandwidth limitations in a system that transfers data across an I/O bus (see, e.g., column 5, lines 37-42, "In summary the system of the invention adds cache storage means and related hardware to a pipeline graphics display system to reduce or eliminate the redundant matrix transformation of shared vertex data, thereby reducing the processing time required to generate the graphics images"). Moreover, Morgan discloses a pipelined architecture and there is no teaching or suggestion in Morgan that bus bandwidth is a concern. In particular, Applicant can find no teaching in Morgan that the bus identified by the Examiner as the I/O bus is of a type that must by acquired by the CPU to implement a data transfer.

Porterfield teaches away from connecting a graphics accelerator to an I/O bus and thus teaches away from Applicant's claimed invention. Porterfield recognizes that a conventional bus has inadequate bandwidth for three dimensional graphics applications but teaches that the solution to the bus bandwidth problem is to directly connect a graphics accelerator to system logic with an accelerated graphics port, as described in column 1, lines 48-51; column 6, lines 33-36; and column 17, lines 22-25. As illustrated in Figure 3 of Porterfield, Porterfield solves the bandwidth issues of conventional buses by directly connecting a graphics accelerator 160 to system logic 154 via an accelerated graphics port (AGP) 166. The Porterfield reference states that the AGP is not a bus and that there is no bus arbitration. As stated in column 6, lines 36-42, of Porterfield "AGP 166 is not a bus, but a point-to-point connection . . . [that] eliminates bus arbitration overhead."

Applicant respectfully submits that the claimed invention distinguishes over the cited prior art. Reconsideration and allowance of the pending claims is respectfully requested.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No 03-3117.

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